IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	Yasuo Inoue
Application No.:	10/614,862
Filed:	July 9, 2003
For:	EXTERNAL STORAGE SUBSYSTEM
Group Art Unit:	2182
Examiner:	Alan S. Chen

COMMUNICATION

Mail Stop - RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto is a Statement of Facts concerning the prior art submitted in the Information Disclosure Statement concurrently filed herewith. If the Examiner has any questions, he is invited to contact the undersigned.

Respectfully submitted,

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Date: July 28, 2005

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Attachment: Statement of Facts

Statement of Facts

1. This application (S/N 10/614,862) is one of six co-pending continuation applications, all claiming priority to the same parent application (S/N 09/819,636). The other co-pending continuation applications are 10/614,859, 10/614,860, 10/614,861, 10/614,863, and 10/614,864.

2. The current 10/614,862 application and the co-pending continuation applications are all entitled to an effective US filing date of December 3, 1992, due to the chain of parent applications of which they claim benefit, and are entitled to a foreign priority date of December 6, 1991, due to the claim for priority under 35 USC 119 from JP 03-322965.

3. US Patent 5,819,054 (hereinafter the '054 patent) is not prior art against the current 10/614,862 application or the co-pending continuation applications, because it has an earliest effective US filing date of June 21, 1994.

4. The inventor of the current application, Yasuo Inoue is a co-inventor of the '054 patent.

5. The '054 patent indicates in the "Description of the Related Art" that JP-B-61-43742 (corresponding to U.S. Pat. No. 4,636,946) discloses a conventional storage system connected to a large-scale computer, and refers to FIG. 20 as a schematic of a conventional storage system, illustrating the connection of host adaptors, host computers, disk adaptors, cache memory, host adaptors and shared management memory.

6. JP-B-61-43742 and U.S. Pat. No. 4,636,946 disclose that the cache and channel adaptor are connected by a common bus, and do not disclose the content of FIG. 20 of the '054 patent.

7. The inventor Yasuo Inoue was involved in preparation of the Japanese priority document, JP 05-162021 from which the '054 patent claims priority. In that Japanese priority document, Inventor Yasuo Inoue mistakenly indicated that JP-B-61-43742 contained these disclosures. This mistake was carried over into filing of the US application that matured into the '054 patent.

8. Inventor Yasuo Inoue should have referred in the '054 patent to JP 03-32965 as disclosing the content described in association with FIG. 20 of the '054 patent. FIG. 20 was derived from Fig. 7 of JP 03-322965, a copy of which is attached (with machine translation).

9. Based on the above facts, FIG. 20 and the associated description of the '054 patent are not prior art against the current 10/614,862 application and the co-pending 10/614,859, 10/614,860, 10/614,861, 10/614,863, and 10/614,864 continuation applications.